

Amendments to the Claims

This listing of claim will replace all prior versions and listings of claim in the application.

- 1 1. (currently amended) An integrated circuit comprising:
 - 2 a control circuit to generate a first control signal according to a phase relationship between
 - 3 an input signal and a first clock signal;
 - 4 a select circuit coupled to receive the first control signal from the control circuit and
 - 5 coupled to receive a second control signal, the select circuit being responsive to a
 - 6 select signal to select ~~either from one of~~ the first control signal ~~or and~~ the second
 - 7 control signal to be output as a selected control signal; and
 - 8 a phase adjust circuit coupled to receive the selected control signal from the select circuit,
 - 9 the phase adjust circuit being responsive to the selected control signal to adjust the
 - 10 phase of the first clock signal.
- 1 2. (previously presented) The integrated circuit of claim 1 further comprising a receive
- 2 circuit to sample the input signal in response to the first clock signal.
- 1 3. (currently amended) The integrated circuit of claim 1 wherein the phase adjust circuit
- 2 includes circuitry to output a plurality of clock signals including the first clock signal, and
- 3 wherein the control circuit comprises:
 - 4 a receive circuit to capture a plurality of samples of the input signal in response to
 - 5 transitions of the plurality of clock signals; and
 - 6 a phase control circuit to determine, based on the plurality of samples of the input signal,
 - 7 whether a transition of the input signal occurs before a transition of the first clock signal
 - 8 and or whether the transition of the input signal occurs after a the transition of the
 - 9 first clock signal.
- 1 4. (currently amended) The integrated circuit of claim 3 wherein the first control signal is a
- 2 digital signal having one of at least two possible states, and wherein the phase control
- 3 signal circuit includes circuitry to output the first control signal in a state selected from one
- 4 of in either a first state or and a second state of the at least two possible states based, at
- 5 least in part, on whether the transition of the input signal occurs before the transition of the

6 first clock signal and or whether the transition of the input signal occurs after the transition
7 of the first clock signal.

1 5. (previously presented) The integrated circuit of claim 1 wherein the first control signal
2 includes a first component signal that is asserted when the first clock signal lags the input
3 signal and a second component signal that is asserted when the first clock signal leads the
4 input signal.

1 6. (previously presented) The integrated circuit of claim 1 wherein the first control signal is
2 an analog signal having a voltage level indicative of the phase relationship between the
3 input signal and the first clock signal.

1 7. (previously presented) The integrated circuit of claim 1 wherein the first control signal is
2 an analog signal having a current level indicative of the phase relationship between the
3 input signal and the first clock signal.

1 8. (previously presented) The integrated circuit of claim 1 further comprising an input to
2 receive the select signal from an external device.

1 9. (currently amended) The integrated circuit of claim 1 further comprising a programmable
2 register to store a mode value, the select signal having either from one of a first state or and
3 a second state according to the mode value, and the select circuit including a circuitry to
4 select the first control signal when the select signal is in the first state and to select the
5 second control signal when the select signal is in the second state.

1 10. (previously presented) The integrated circuit of claim 1 wherein the select circuit
2 comprises a multiplexer circuit.

1 11. (currently amended) A method of operation within an integrated circuit, the method
2 comprising:
3 determining a phase relationship between an input signal and a first clock signal;
4 generating a first control signal according to the phase relationship between the input signal

5 and the first clock signal;
6 selecting either from one of the first control signal or and a second control signal to be
7 output to a phase adjust circuit as a selected control signal; and
8 adjusting, in the phase adjust circuit, a phase of the first clock signal according to the
9 selected control signal.

1 12. (previously presented) The method of claim 11 further comprising sampling the input
2 signal in response to the first clock signal.

1 13. (currently amended) The method of claim 11 further comprising:
2 outputting a plurality of clock signals, including the first clock signal;
3 capturing a plurality of samples of the input signal in response to transitions of the plurality
4 of clock signals; and
5 determining the phase relationship between the input signal and the first clock signal, at
6 least in part, by determining, based on the plurality of samples of the input signal,
7 whether a transition of the input signal occurs before a transition of the first clock
8 signal and or whether the transition of the input signal occurs after a the transition of
9 the first clock signal.

1 14. (currently amended) The method of claim 13 wherein generating the first control signal
2 comprises generating a digital control signal having one of at least two possible states
3 based, at least in part, on whether the transition of the input signal occurs before the
4 transition of the first clock signal and or whether the transition of the input signal occurs
5 after the transition of the first clock signal.

1 15. (previously presented) The method of claim 11 wherein generating the first control signal
2 comprises generating a digital signal having a first and second component signals, the first
3 component signal being asserted when the first clock signal lags the input signal and the
4 second component signal being asserted when the first clock signal leads the input signal.

1 16. (previously presented) The method of claim 11 further comprising receiving the selected
2 control signal from a device that is external to the integrated circuit.

- 1 17. (previously presented) The method of claim 11 further comprising storing a mode value in
2 a programmable register within the integrated circuit, and wherein generating the selected
3 control signal comprises generating the selected control signal according to the mode
4 value.
- 1 18. (previously presented) The method of claim 11 further comprising
2 receiving a command to store a mode value; and
3 storing the mode value in a register within the integrated circuit; and
4 wherein generating the selected control signal comprises generating the select signal
5 according to the mode value.
- 1 19. (currently amended) An integrated circuit device comprising:
2 a first clock data recovery (CDR) circuit to recover clock and data signals from a first
3 signal line, the first CDR circuit including:
4 a first phase control circuit to generate a first control signal, and
5 a first phase adjust circuit to adjust the phase of a first recovered clock signal in
6 response to the first control signal; and
7 a second CDR circuit to recover clock and data signals from a second signal line, the
8 second CDR circuit including:
9 a second phase control circuit to generate a second control signal,
10 a select circuit coupled to receive the first and second control signals and being
11 responsive to a select signal to select either from one of the first control signal
12 or and the second control signal to be output as a selected control signal, and
13 a second phase adjust circuit to adjust the phase of a second recovered clock signal in
14 response to the selected control signal.
- 1 20. (currently amended) The integrated circuit device of claim 19 wherein the select circuit
2 comprises a multiplexer circuit having a control input coupled to receive the selected
3 control select signal and having respective input ports coupled to receive the first and
4 second control signals from the first and second phase control circuits.

- 1 21. (currently amended) The integrated circuit device of claim 19 further comprising
2 additional CDR circuits each having a respective phase control circuit, select circuit and
3 phase adjust circuit, the select circuit of each of the additional CDR circuits being
4 responsive to a control input to output, as a selected control signal, either from one of the
5 first control signal or and a phase control signal output by the phase control circuit of the
6 additional CDR circuit, the phase adjust circuit of each of the additional CDR circuits
7 being responsive to the selected control signal output by the select circuit for the additional
8 CDR circuit to adjust the phase of a respective recovered clock signal.
- 1 22. (previously presented) The integrated circuit device of claim 19 wherein the first CDR
2 circuit further includes a first receive circuit to sample an input signal on the first signal
3 line in response to the first recovered clock signal, and the second CDR circuit further
4 includes a second receive circuit to sample an input signal on the second signal line in
5 response to the second recovered clock signal.
- 1 23. (previously presented) The integrated circuit device of claim 19 further comprising an
2 input to receive the select signal from an external device.
- 1 24. (currently amended) The integrated circuit device of claim 19 further comprising a
2 programmable register to store a mode value, the select signal having either from one of a
3 first state or and a second state according to the mode value, and the select circuit including
4 a circuitry to select the first control signal when the select signal is in the first state and to
5 select the second control signal when the select signal is in the second state.
- 1 25. (previously presented) The integrated circuit device of claim 19 wherein the select circuit
2 is responsive to the select signal to disable generation of the first control signal when the
3 select signal indicates that the select circuit is to select the second control signal to be
4 output as the selected control signal.
- 1 26. (currently amended) A method of controlling an integrated circuit, the method comprising:
2 outputting a first command to the integrated circuit to set a first clock data recovery (CDR)

3 circuit within the integrated circuit to a first mode, the first CDR circuit including a
4 select circuit to select a first control signal to adjust the phase of a first clock signal
5 when the first CDR circuit is in the first mode;
6 delaying for a first time interval; and
7 outputting, after the first time interval, a second command to the integrated circuit to set the
8 first CDR circuit to a second mode, the select circuit of the first CDR circuit ~~being~~
9 adapted to select a second control signal when the first CDR circuit is in the second
10 mode, the second control signal being generated by a second CDR circuit.

1 27. (previously presented) The method of claim 26 wherein delaying for the first time interval
2 comprises delaying until a predetermined number of cycles of a clock signal have
3 transpired.

1 28. (previously presented) The method of claim 26 wherein outputting the first command to
2 the integrated circuit to set the first CDR circuit to the first mode comprises outputting a
3 command to the integrated circuit to store a mode value in a programmable register within
4 the integrated circuit, the mode value indicating the first mode.

1 29. (previously presented) The method of claim 26 wherein outputting the first command to
2 the integrated circuit to set the first CDR circuit to the first mode comprises outputting a
3 mode signal to the integrated circuit, the mode signal being input to a select input of the
4 select circuit to select the first control signal.

1 30. (previously presented) The method of claim 26 further comprising periodically repeating
2 the outputting the first command to the integrated circuit, delaying for the first time
3 interval, and outputting the second command to the integrated circuit.

1 31. (previously presented) The method of claim 26 further comprising:
2 detecting a predetermined condition; and
3 in response to the detecting the predetermined condition, repeating the outputting the first
4 command to the integrated circuit, delaying for the first time interval, and outputting
5 the second command to the integrated circuit.

- 1 32. (previously presented) The method of claim 31 wherein the detecting the predetermined
2 condition comprises detecting a change in temperature.
- 1 33. (previously presented) The method of claim 31 wherein the detecting the predetermined
2 condition comprises detecting a change in voltage.
- 1 34. (previously presented) The method of claim 31 wherein the detecting the predetermined
2 condition comprises detecting a loss of synchronization between the first clock signal and a
3 data signal received in the first CDR circuit.
- 1 35. (currently amended) A system comprising:
2 a first signal line;
3 a receive device coupled to the first signal line, the receive device having a first clock data
4 recovery (CDR) circuit to recover clock and data signals from the first signal line, the
5 first CDR circuit including a control circuit, a select circuit and a phase adjust circuit,
6 the control circuit ~~being adapted~~ to generate a first control signal according to a phase
7 relationship between an input signal on the first signal line and a first clock signal, the
8 select circuit being responsive to a first mode value to select ~~either~~ from one of the
9 first control signal ~~or~~ and a second control signal to be output as a selected control
10 signal, the phase adjust circuit ~~being adapted~~ to adjust the phase of the first clock
11 signal according to the selected control signal; and
12 a control device coupled to the receive device to provide the first mode value ~~thereto~~.
- 1 36. (previously presented) The system of claim 35 wherein the control device is coupled to
2 provide the first mode value to the receive device via the first signal line.
- 1 37. (currently amended) The system of claim 35 further comprising at least one additional
2 signal line, the at least one additional signal line ~~being~~ coupled to the receive device and to
3 the control device, the control device ~~being adapted~~ to provide the first mode value to the
4 receive device via the at least one additional signal line.

- 1 38. (currently amended) The system of claim 35 wherein the control device ~~is adapted~~ to
2 output the first mode value to the receive device and then, after a first time interval, to
3 output a second mode value to the receive device, the select circuit being responsive to the
4 first mode value to select the first control signal to be output as the selected control signal,
5 the select circuit being responsive to the second mode value to select the second control
6 signal to be output as the selected control signal.
- 1 39. (previously presented) The system of claim 38 further comprising a second signal line
2 coupled to the receive device, and wherein the receive device includes a second CDR
3 circuit to recover clock and data signals from the second signal line, the second CDR
4 circuit including a control circuit to generate the second control signal according to a phase
5 relationship between an input signal on the second signal line and a second clock signal.
- 1 40. (previously presented) The system of claim 35 wherein the receive device is implemented
2 in a first integrated circuit and the control device is implemented in a second integrated
3 circuit.
- 1 41. (previously presented) The system of claim 40 wherein the first and second integrated
2 circuits are packaged in separate integrated circuit packages.
- 1 42. (previously presented) The system of claim 40 wherein the first and second integrated
2 circuits are packaged in the same integrated circuit package.
- 1 43. (previously presented) The system of claim 35 wherein the receive device and the control
2 device are implemented within a single integrated circuit.
- 1 44. (cancelled)
- 1 45. (currently amended) A method of testing an integrated circuit (IC) that includes a clock
2 data recovery (CDR) circuit and a phase control port, the method comprising:
3 outputting a ~~first~~ command to the IC to set the CDR circuit to a ~~first mode~~ of operation, the

4 CDR circuit having a select circuit that responds to the first mode of operation by
5 selecting the phase control port to source a control signal instead of a phase control
6 circuit within the CDR circuit, the control signal being used by a phase adjust circuit
7 within the CDR circuit to adjust the phase of a first clock signal;
8 outputting a phase control signal to the phase control port of the integrated circuit device to
9 adjust the phase of the first clock signal; and
10 wherein outputting the first command to the integrated circuit to set the CDR circuit to the
11 first mode of operation comprises outputting a command to the integrated circuit to
12 store a mode value in a programmable register within the integrated circuit, the mode
13 value indicating the first mode of operation.

- 1 46. (cancelled)
- 1 47. (currently amended) A method of testing an integrated circuit (IC) that includes a clock
2 data recovery (CDR) circuit and a phase control port, the method comprising:
3 a. outputting a first command to the IC to set the CDR circuit to a first mode of operation, the
4 CDR circuit having a select circuit that responds to the first mode of operation by
5 selecting the phase control port to source a control signal instead of a phase control
6 circuit within the CDR circuit, the control signal being used by a phase adjust circuit
7 within the CDR circuit to adjust the phase of a first clock signal;
8 b. asserting a phase control signal at the phase control port of the integrated circuit for a first
9 predetermined time interval, the phase adjust circuit within the CDR circuit being
10 responsive to the phase control signal to adjust the phase of the first clock signal;
11 e. deasserting the phase control signal for a second predetermined time interval; and
12 d. measuring the first clock signal with a signal measuring device while repeating steps b and
13 e asserting a phase control signal and deasserting the phase control signal at least
14 until the phase of the first clock signal has progressed through a predetermined
15 portion of a cycle of the first clock signal.
- 1 48. (currently amended) The method of claim 47 wherein the predetermined portion of a cycle
2 of the first clock signal is an entire cycle of the first clock signal.

- 1 49. (currently amended) The method of claim 47 wherein the phase adjust circuit responds to
2 assertion of the control signal by advancing the phase of the ~~first~~ clock signal.
- 1 50. (currently amended) The method of claim 47 wherein the first predetermined time interval
2 is selected to allow the phase adjust circuit to advance the phase of the ~~first~~ clock signal by
3 a predetermined phase angle.
- 1 51. (currently amended) The method of claim 47 wherein measuring the ~~first~~ clock signal with
2 a signal measuring device comprises measuring the ~~first~~ clock signal with an oscilloscope.
- 1 52. (currently amended) An integrated circuit device comprising:
2 a first signal generator to generate a first test signal;
3 a receive circuit having an input switchably coupled to receive the first test signal from the
4 first signal generator, the receive circuit including circuitry responsive to a first clock
5 signal to capture samples of the first test signal;
6 a clock data recovery (CDR) circuit having a control circuit, a select circuit and a phase
7 adjust circuit, the control circuit ~~being adapted~~ to generate a first control signal based
8 on the samples of the first test signal, the select circuit ~~being~~ responsive to a select
9 signal to select ~~either~~ from one of the first control signal ~~or~~ and a second control
10 signal to be output as a selected control signal, and the phase adjust circuit ~~being~~
11 responsive to the selected control signal to adjust the phase of the first clock signal;
12 and
13 a compare circuit to compare the samples of the first test signal to a compare signal.
- 1 53. (previously presented) The integrated circuit device of claim 52 wherein the first signal
2 generator is a linear feedback shift register and the first test signal is a pseudo random bit
3 sequence.
- 1 54. (currently amended) The integrated circuit device of claim 52 further comprising a
2 transmit circuit having an input and an output, the input of the transmit circuit ~~being~~
3 switchably coupled to receive the first test signal from the first signal generator, and the

4 output of the transmit circuit being switchably coupled to the input of the receive circuit.

1 55. (previously presented) The integrated circuit device of claim 52 further comprising a mode
2 control circuit to store a mode value indicative of an operating mode of the integrated
3 circuit device, the mode control circuit outputting a test mode signal when the mode value
4 is indicative of a test mode of operation, the test mode signal switching the input of the
5 receive circuit to be coupled to receive the first test signal.

1 56. (previously presented) The integrated device of claim 52 wherein the compare circuit
2 includes a second signal generator to generate the compare signal.

1 57. (previously presented) The integrated circuit device of claim 56 wherein the first signal
2 generator and the second signal generator are designed to generate identical signals.

1 58. (previously presented) The integrated device of claim 52 wherein the first signal generator
2 is coupled to provide the first test signal to the compare circuit, the compare signal being
3 the first test signal.

1 59. (currently amended) A method of testing an integrated circuit that includes a clock data
2 recovery (CDR) circuit and a phase control port, the method comprising:

- 3 a. setting the CDR circuit to a test mode in which a select circuit within the CDR circuit
4 selects the phase control port to source a control signal instead of a phase control
5 circuit within the CDR circuit, the control signal being used by a phase adjust circuit
6 within the CDR circuit to adjust the phase of a first clock signal;
- 7 b. inputting a test signal to a receiver of the CDR circuit;
- 8 c. comparing the test signal against samples of the test signal generated by the CDR circuit;
- 9 d. asserting an error signal when the test signal does not match the samples;
- 10 e. asserting a phase control signal at the phase control port to adjust the phase of the first
11 clock signal; and
- 12 f. repeating steps c through e comparing the test signal, asserting an error signal and asserting
a phase control signal to determine a maximum phase and a minimum phase of the
13 first clock signal for which the error signal is not asserted.